A Novel Orthogonal Gate EDMOS Transistor
With Improved $dv/dt$ Capability and Figure of Merit (FOM)

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Abstract—A transistor with an orthogonal gate (OG) electrode is proposed to improve $dv/dt$ capability, reduce the gate-to-drain overlap capacitance ($C_{gd}$), and improve figure of merit (FOM). The OG has both a horizontal section and a vertical section for MOS gate control. This 30 V device is implemented in a 0.18 μm CMOS compatible process. Comparing to a conventional extended drain MOSFET transistor with the same voltage rating and device size, four times higher $dv/dt$ capability and 53% improvement in FOM are observed.

Index Terms—$dv/dt$ capability, extended drain MOSFETs (EDMOS), figure of merit (FOM), gate-to-drain capacitance, orthogonal gate (OG).

I. INTRODUCTION

The POWER semiconductor industry has achieved rapid progress in the reduction of specific on-resistance ($R_{on,sp}$) and improvement of breakdown voltage in power MOSFETs, particularly in the low voltage range such as 30 V rating for display driver or DC–DC converter applications [1]. Extended drain MOSFET (EDMOS) is particularly attractive in these applications. However, only focusing on breakdown and specific on-resistance relationship is not enough for modern power devices; thus, $dv/dt$ capability of power MOSFETs should also be considered. Since the power MOSFETs are widely used as on–off switches, the $dv/dt$ capability of power MOSFETs determines the overall reliability. In this letter, we propose an EDMOS transistor with a novel orthogonal gate (OG) electrode designed to provide high $dv/dt$ capability, fast switching speed, low gate charge, and reduced $R_{on,sp}$. The device structure and the fabrication processes are described, and the device characterization results are presented.

II. DEVICE STRUCTURE AND FABRICATION

The OG-EDMOS transistor fabrication process is based on a 0.18 μm high voltage (HV) CMOS technology developed by Asahi Kasei EMD. Both HV devices (30 V n- and p-type EDMOS transistors) and standard CMOS are available in this technology.

Fig. 1. Cross-sectional view of the OG EDMOS and conventional gate EDMOS transistors.
lithography and etch, gate oxidation, polysilicon deposition, polysilicon gate etch, and doping annealing are then carried out to form the gate electrode. The gate mask is then used to define the entire OG electrode. Thereafter, a thick interlevel oxide deposition of TEOS is followed by contact lithography and oxide etching to form the contact window. Finally, metallization and passivation are carried out to complete the EDMOS transistor fabrication sequence. The cross-sectional diagram of the device is illustrated in SEM micrograph shown in Fig. 2.

III. CHARACTERIZATION AND DISCUSSION

The OG-EDMOS transistor achieved a breakdown voltage of 35.2 V and $R_{on,sp} = 32.4$ mΩ·mm² at $V_{gs} = 5$ V and $V_{ds} = 1$ V, respectively. The electrical characteristics of both the fabricated OG and conventional gate EDMOS transistors are compared in Table I. The specific on-resistance is reduced by 24% due to the reduction of lateral channel length $A$ (see Fig. 1). The OG-EDMOS drift region is completely underneath the STI; this reduces the risk of punch through between the drift region and the source. The minimum lateral channel length $A_1$ is 0.3 μm in OG-EDMOS before punch-through breakdown would occur. As a result, we can reduce channel length from $A_2 = 1$ μm to $A_1 = 0.3$ μm. Since the STI depth is 0.35 μm, the total channel length is estimated to be $0.3 + 0.35 = 0.65$ μm for the OG-EDMOS. As the effective channel length is reduced, the total on-resistance is also lowered for the OG-EDMOS.

One of most prominent features of the OG-EDMOS transistor is a reduction in $C_{gd}$ due to the minimization of the gate-to-drain overlap capacitance [4]. The gate trench opening width is 0.2 μm, and there is no vertical sidewall overlap between gate and drain. Comparing to a conventional EDMOS transistor with the same voltage rating and device size, 75% and 88%...
reductions in $C_{gd}$ are observed at $V_{ds} = 0$ V for n-type and p-type OG-EDMOS, respectively (see Fig. 3).

The transient $\frac{dv}{dt}$ capability is defined as the maximum rate of rise in drain–source voltage without causing inadvertent turn-on of the transistor, $\frac{dv}{dt} = \frac{v_{th}}{R_g C_{gd}}$. If this rate exceeds a certain value, the voltage across the gate–source terminals may become higher than the threshold voltage, turning on the device (see Fig. 4). Moreover, in extreme cases, catastrophic failure may occur. Therefore, $\frac{dv}{dt}$ capability is an important reliability characteristic. For devices at a given voltage rating, higher $\frac{dv}{dt}$ capability is more desirable. From the $\frac{dv}{dt}$ simulation comparison as shown in Fig. 5, the OG-EDMOS transistor demonstrates four times higher $\frac{dv}{dt}$ capability for transistors with threshold voltage $=1$ V.

The comparison of gate charge ($Q_g$) between the OG and conventional gate EDMOS transistors is presented in Fig. 6, where $Q_g$ specifies the amount of gate charge required to drive the MOSFET gate-to-source voltage ($V_{gs}$) from 0 to 10 V. It is obtained by integrating the gate current as a function of time, $Q_g = \int I_g \cdot dt$. The OG-EDMOS transistor demonstrates a 37.5% reduction in total $Q_g$ at $V_{gs} = 10$ V.

IV. CONCLUSION

In summary, an orthogonal gate structure has been developed for EDMOS transistor. The fabrication process is based on a 0.18 $\mu$m CMOS compatible technology. The breakdown voltage and on-resistance are comparable with conventional EDMOS transistors. The proposed OG-EDMOS transistor achieved four times higher $\frac{dv}{dt}$ capability, 75% reduction in $C_{gd}$ for n-type OG-EDMOS, 88% reduction in $C_{gd}$ for p-type OG-EDMOS, 24% reduction in $R_{on,sp}$, and 53% improvement in FOM without degradation in breakdown voltage or on-resistance. The enhanced performance of the OG-EDMOS will translate into better power conversion efficiency with higher reliability when employed in switched mode power supply applications.

REFERENCES