A 38W Digital Class D Audio Power Amplifier Output Stage with Integrated Protection Circuits

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Abstract—This paper presents an integrated digital class D audio power amplifier output stage implemented in a 40V, 0.35µm HV-CMOS technology. The integrated output stage consists of a full H-bridge, gate drivers, bootstrap diodes and protection circuits. Its performance was found to be better than previously published output stages implemented in SOI based BCD processes, which are typically more complex and costly. Experimental results show that low distortion is achieved with high efficiency. In open loop configuration, the minimum Total Harmonic Distortion plus Noise (THD+N) was measured to be 0.016%. The output stage has a maximum efficiency of 88% and delivers up to 38W into a 4Ω Bridge-Tied Load (BTL).

I. INTRODUCTION

Typical class D amplifiers use a PWM modulator to drive the output stage in an open-loop configuration. The modulator can be digital or analog. The digital modulator has a cost advantage when implemented in submicron CMOS technology. In addition, the digital signal path provides high noise immunity for the entire system. However, the audio quality is usually not as good as its analog counterpart, the Total Harmonic Distortion plus Noise (THD+N) is typically 0.1% or worse [1].

This paper presents a 38W digital class D audio power amplifier output stage. Driven by a prototype digital modulator AK47302, the output stage achieves very low distortion with high efficiency. Furthermore, the output stage is implemented in a simple HV-CMOS technology, which offers further cost savings.

II. DESIGN CONSIDERATIONS

The design considerations for the class D amplifier output stage are discussed in this section.

1) Power Efficiency: The primary sources of power loss in the output stage are the power MOSFET conduction loss, gate drive loss and switching loss. The peak efficiency η_peak is primarily determined by the conduction loss. Equation (1) provides a first order estimate for the R_on required to achieve certain peak efficiency, where k is a variable that accounts for the gate drive loss and switching loss and k is typically between 5% to 8%.

\[ \eta_{\text{peak}} = \frac{R_{\text{on}}}{R_{\text{on}} + 2 R_{\text{on}} - k} \]  

(1)

2) Distortion: It has been shown that dead time is one of the major sources of distortion in class D audio power amplifiers [2]. As a result, very short to no dead time is typically used in class D audio power amplifiers. In addition, the routing resistance in series with the power MOSFET’s source terminal should also be minimized. This resistance changes the gate to source voltage when current varies, causing R_on to fluctuate. The power MOSFET’s turn-on/off time also has influence on the distortion level.

3) Reliability: Output stages are operated under high stress conditions involving large amount of voltage, current and heat. To prevent premature failures, electromigration and latchup issues must be considered as an important part of the design.

III. OUTPUT STAGE DESIGN AND LAYOUT

The 38W digital class D audio power amplifier output stage is implemented using a 40V, 0.35µm HV-CMOS technology [3]. This technology was developed based on a 0.35µm CMOS process with only 5 additional masking layers, and provides a simpler platform to implement Power Integrated Circuits (PIC). The floating source n-channel EDMOS exhibits both low on-resistance and high blocking voltage, while the characteristics of the standard CMOS remain unchanged. There are four layers of metal in this technology.

The output stage employs n-channel floating source EDMOS transistors in an H-Bridge configuration. The high side gate driver is supplied by a bootstrap circuit (see Fig. 1). The load is connected in a mono Bridge-Tied Load (BTL) configuration. The external LC filter and bootstrap capacitors are also shown in Fig. 1.

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2. Product under development, Asahi Kasei EMD Corporation, Japan.
The digital modulator used is a prototype version of AK 4730, and it was implemented using a standard 0.35µm CMOS process. The digital modulator accepts standard I2S audio signals and provides PWM driving signals for the output stage. The PWM switching frequency is 384 kHz and the DPWM resolution is 8 bits.

A. Power MOSFET Design and Layout

In order to obtain a peak efficiency of 90% for an 8 Ω BTL load, power MOSFET with Ron of 200 mΩ is required. The power MOSFET is sized to have a W/L ratio of 75000, which corresponds to 138 mΩ on-resistance according to SPICE simulation. This leaves 62 mΩ for the routing and packaging resistance. The die area required for each power MOSFET is approximately 0.6 mm².

1) The Power Transistor Array: The power MOSFET is laid out as an array of unit cells (see Fig. 2). Each power MOSFET is built from 256 (row) \times 31 (column) unit transistors. The columns are grouped into sets of 11, 10, and 10 in order to make room for two columns of poly gate contacts. Each source and drain are connected in three layers of metal to reduce resistance.

To achieve the most compact layout, the minimum allowed dimensions are used in the unit cell design whenever possible. The gate width of the unit cell transistor is selected based on switching speed consideration, which is determined by τgate. This time constant is due to the gate resistance and capacitance, both of which increase with the gate width. Using (2) [4], τgate can be estimated, where R and C are the total gate resistance and capacitance, r and c are the per-unit-width resistance and capacitance, and W is the gate width.

\[
\tau_{gate} = 0.9 RC = 0.9rcW^2 
\]  

(2)

It is determined that a τgate of 5ns or lower is needed, which can be achieved if the unit gate width is below 90 μm. It can be shown that a longer gate width makes the layout more compact, therefore the longest possible width permitted by the speed requirement should always be used. Nevertheless some margin of safety has to be added since (2) is only a first order estimate and is very sensitive to W.

2) Layout Techniques to Reduce Routing Resistance: The routings in series with the power MOSFET’s drain and source are done using three layers of metal. The bonding pads are placed directly over the power MOSFET to reduce routing resistance (see Fig. 2).

3) Layout for Reliability: A number of latchup prevention steps are taken. To achieve high substrate contact density, columns of substrate contacts are embedded in the source regions, as shown in Fig. 2. Further reduction in substrate current injection is realized by isolating each power MOSFET in its own n-Well, and forming isolation rings around all circuit structures.

B. Gate Driver Design

1) Low-Side Driver: A power efficient low-side gate driver design is shown in Fig. 3. Dead time is introduced to the PWM waveforms in order to guard against high shoot through current. For this reason, the pull-up and pull-down transistors in the final stage are driven by two different inverter chains. A stage effort of 8 is used and it has been determined to be sufficiently strong to achieve an output rise and fall time under 5ns. The dead time period is kept to a minimum because too much dead time results in signal dependent distortion [2]. The digital modulator chip has the ability to produce additional adjustable dead time if necessary.

![Figure 1. Output stage PIC block diagram and the H-bridge components.](image1)

![Figure 2. Power MOSFET layout arrangement and isolation structure.](image2)

![Figure 3. Low side gate driver.](image3)
A bootstrap circuit is used to provide this voltage. Its gate voltage must be driven sufficiently high above $V_{DS}$ when $V_{SW}$ is low, and maintains $V_{DS}$ to be higher than $PVDD$ when $V_{SW}$ is high. The high side gate driver’s pull-down network is connected to $V_{DS}$, and its pull-up network is connected to $V_{SW}$. This allows the gate to source voltage to be set to either 0 or $V_{SW}=V_{DS}$ depending on the logic state of the driver. The circuit schematics of the dead time generator, delay cell and level shifter are as shown in Fig. 5. The dead time generator uses area efficient current-starved delay cells. The level shifter circuit is able to upconvert the input from $V_{DD}$ to $PVDD$.

Delay Matching: The same gate driver topology is used for both the low-side and high-side in order to match the propagation delay. This is important to avoid shifting the PWM pulse center alignment and consequently introduces distortion.

IV. PROTECTION CIRCUITS

A. Over Temperature(O.T.) Protection

Temperature sensing is achieved by comparing the temperature independent voltage reference $V_{ref}$ to the Proportional-To-Absolute-Temperature (PTAT) voltages. The circuit is designed such that $V_{ref}, V_{warn}$ and $V_{err}$ exceed $V_{ref}$, when the chip temperature goes above 100°C, 125°C, and 150°C respectively.

B. Over Current(O.C.) Protection

A simple and effective current detection scheme based on $V_{DS}$ sensing [5] is used in this work to provide over current protection.

V. TESTING RESULTS

The micrograph of the output stage is shown in Fig. 7(a). The die area is 2.8 mm × 3.4 mm. Bonding wires are directly connected to pads embedded in power MOSFETs. The bootstrap diodes are also integrated on chip to reduce external component count.

A prototype PCB for the output stage is shown in Fig. 7(b). The output stage is connected in a mono BTL configuration. With a supply voltage of 25V, the output stage can deliver up to 38W into a 4 Ω BTL load. Fig. 8 shows the THD+N versus output power plot for a 1 kHz input signal with dead time of 20 ns and 0 ns. The minimum THD+N is measured to be 0.016%, which is significantly lower than 0.034% reported by Berkhout [6].

The measurements were performed using an Audio Precision SYS-2522 audio analyzer with AES 17 filter option in conjunction with AP AUX-0025 Switching Amplifier Measurement Filter.
A maximum efficiency of 88% is achieved with an 8 Ω BTL load, as shown in Fig. 9. The O.C. protection circuit was tested by generating a short condition at the load. The response time of 50 ns was found to be sufficiently fast to protect the output stage (see Fig. 10).

The PIC die is housed in a Power SOP3 package for better heat dissipation. The package was exposed to an external heat source during O.T. testing. The O.T. protection circuit was found to be triggered at a case temperature of 100 °C and deactivated itself at 90 °C due to built-in hysteresis control (see Fig. 10). Other parameters of the output stage are summarized in Table I.

### Table I. Performance Summary.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Typical Values</th>
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<tbody>
<tr>
<td>Power switch on-resistance</td>
<td>280 mΩ</td>
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<tr>
<td>Power stage supply voltage</td>
<td>25 V</td>
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<tr>
<td>Max power (4 Ω load)</td>
<td>38 W</td>
</tr>
<tr>
<td>Over current response time</td>
<td>50 ns</td>
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<tr>
<td>Over temperature</td>
<td>100 °C</td>
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<tr>
<td>System efficiency</td>
<td>88 %</td>
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<tr>
<td>Switching frequency</td>
<td>384 kHz</td>
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<tr>
<td>DPWM resolution</td>
<td>8 bits</td>
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<tr>
<td>Power stage prop. delay</td>
<td>28 ns</td>
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<tr>
<td>Power stage rise/fall time</td>
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<tr>
<td>Quiescent current</td>
<td>29 mA</td>
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<tr>
<td>Best THD+N</td>
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<td>Chip size</td>
<td>9.71 mm²</td>
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<tr>
<td>Package</td>
<td>Power SOP3</td>
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</table>

### Conclusion

A digital class D audio power amplifier output stage with protection circuits has been presented. Without using the expensive SOI based BCD process, the output stage achieved excellent THD+N and high efficiency. Low distortion is achieved using minimum dead time, matched propagation delay of the gate driver and optimized power MOSFET switching speed. This is a promising approach for amplification of modern digital form factor media having high quality musical content.

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### References


